

A Second Channel between Cache and Memory For Decreased Queuing Delay

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 Reference: Secondary Bus

Inventors



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Overview

Auburn University seeks a licensee or development partner for an invention that improves overall computer system speed by 5-30% by decreasing queuing delay on the primary bus by 75-90% and decreasing requests to primary bus by 30%. This is accomplished by introducing a second channel to commit write-back buffer whenever the system bus is busy with Input/Output operations. This technology substantially enhances system real-time performance and (temporal) determinacy.

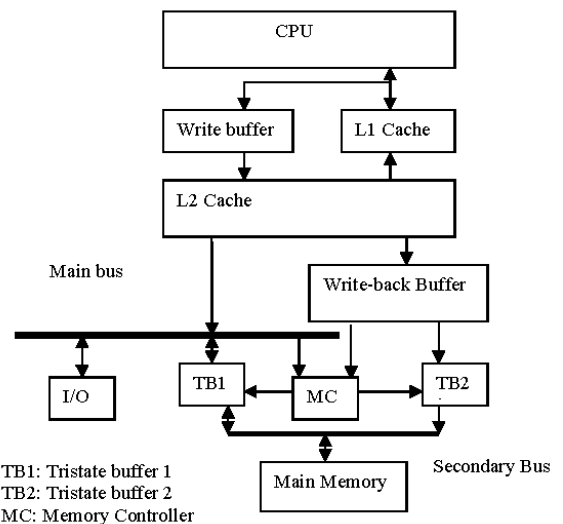
Description

This invention introduces a secondary channel between the main memory and write-back buffer through the main bus. This secondary channel commits write-back buffer when the bus is busy performing input/output operations while the memory remains idle. By parallelizing input/output and memory operations, queuing delays are reduced. Simulation results show that overall system speed is increased by 5-30% along with a substantial decrease in queuing delays.

This secondary channel invention can be implemented by a serial line connecting the cache and memory, or by adding wireless communication capabilities such as the evolving wireless super-connect to transfer data between cache and memory modules¹.

Key features:

- Speeds up system by 5-30% by reducing queuing delays on the primary bus
- Parallelizes input/output and memory operations which results in improving overall performance of the system
- Substantially enhances real-time performance and temporal determinacy by reducing queuing delays on the primary bus
- Valuable for input/output intensive as well as graphics intensive applications (e.g., printer controllers, medical imaging)



Schematic of proposed system architecture

TB1: Tristate buffer 1
 TB2: Tristate buffer 2
 MC: Memory Controller

Status

- Software-based simulation of system performance has been conducted
- Design of memory controller to support the added function has been completed
- A patent application has been filed

Licensing Opportunities

- Available for exclusive or "sign and send" non-exclusive licensing
- Joint development opportunities include funded research or collaborative efforts to pursue implementation for further testing

¹N. Miura, D. Mizoguchi, T. Sakurai, and T. Kuroda, "Analysis and Design of Inductive Coupling and Transceiver Circuit for Inductive Inter-Chip Wireless Superconnect", *IEEE Journal of Solid State Circuit*, Volume 40, Issue 4, pp. 829-837, April 2005.

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