Samuel Ginn College of Engineering

Auburn University

Estimating Reliability of Components for IC Testing and Quality Optimization

Contact

Brian Wright
Auburn University
Office of Technology Transfer
334-844-4977
brian.wright@auburn.edu
http://ott.auburn.edu/
Reference: Reliability Testing

Inventors

Dr. Adit D. Singh
James B. Davis Professor
Department of Electrical and Computer Engineering

Dr. Thomas S. Barnett
Ph.D. Graduate
Department of Electrical and Computer Engineering

References

- "Extending integrated circuit yield models to estimate early-life reliability," *IEEE Transactions on Reliability*, Sept. 2003.
- "Yield-reliability modeling: experimental verification and application to burn-in reduction," VLSI Test Symposium, 2002.

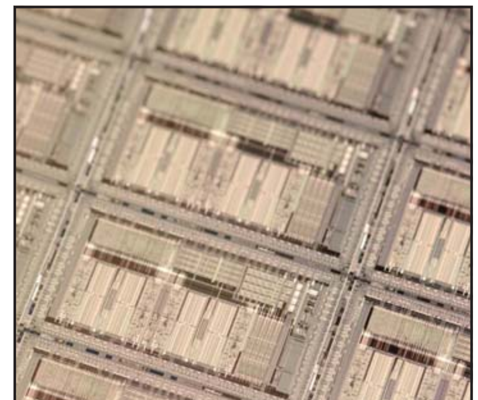
Click here **for a listing of Auburn's available physical science technologies**

Auburn University is an equal opportunity educational institution/employer

Overview

Auburn University seeks a licensee or development partner for an invention that tests integrated circuit (IC) reliability while optimizing quality and cost. This methodology selectively reduces reliability tests without sacrificing quality. It has potential applications in electronic component manufacturing and testing, including IC fabrication.

Advantages



- Determines early mortality of ICs
- Optimizes testing cost and time
- Adapts burn-in test intensity to the probability of defect level in the chip
- Facilitates reliability screening of a die that cannot be stress tested

Description

In integrated circuit (IC) manufacturing, a chip may acquire two types of defects: killer and latent. Killer defects are simple to detect using commonly known wafer probe tests. Our invention provides a cost effective way to identify latent defects.

This methodology is founded on the fact that manufacturing defects tend to cluster in scattered regions of the wafer, and on the related proven assumption that the probability of defects in a die correlates with the defect rate in neighboring dies.

The probability that a given chip has a latent defect is calculated based on the number of neighboring components found to have killer defects. Chips can be divided into groups ("bins") based on this probability. Subsequent burn-in tests or stress tests are adapted to suit the probability of defects associated with each bin — that is, contents of some bins are tested less than others to minimize the overall cost of testing without reducing the reliability of the end product.

For instance, a shorter burn-in time may be used when testing components from a bin that is statistically less likely to have latent defects, or intensive burn-ins may be used with memory chips in a bin that require a greater number of redundant memory repairs.

This selective testing reduces costly and unnecessary intensive testing with no compromise in reliability or quality. In addition, Multi Chip Modules (MCMs) made from chips with low defect probability may not require testing after assembly, yielding additional cost savings.

Status

- Subject of United States Patents 7,194,366 and 7,409,306
- This invention has been successfully verified by simulation and laboratory experiment

Licensing Opportunities

- This technology is available for exclusive or non-exclusive licensing
- Joint development opportunities exist