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High Order $\Delta\Sigma$ Noise Shaping in Direct Digital Synthesis

Contact

Brian Wright
Auburn University
Office of Technology Transfer
334-844-4977
brian.wright@auburn.edu
<http://ott.auburn.edu/>
Reference: Delta Sigma

Inventor



Dr. Foster Dai
Associate Professor
Department of Electrical
and Computer Engineering

Reference

[1] Dai, Ni, Yin and Jaeger,
*IEEE Journal of Solid-State
Circuits*, vol. 41, no. 4, pp.
839-850, April 2006. ([Read](#))

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Overview

This invention embodies a novel direct digital synthesis (DDS) architecture using high-order $\Delta\Sigma$ interpolators to remove frequency, phase and amplitude domain quantization errors. The presented DDS can achieve very low phase noise with ultra fine frequency resolution, and thus provides a low cost and high performance means of frequency synthesis. This technology has potential applications in wireless, satellite and military communications.

Advantages

- Achieves ultra low phase noise DDS frequency synthesis approaching that of PLL-based analog synthesizers
- Achieves fine frequency resolution, improving communication and scanning capabilities
- Uses high-order $\Delta\Sigma$ interpolators to remove frequency, phase and amplitude domain quantization errors
- Reduces the DDS ROM size without degradation, while maintaining large Spurious Free Dynamic Range (SFDR) and fine resolution
- Easy to implement in digital CMOS processing
- Could allow DDS to replace more expensive analog synthesizers

Description

Conventional analog frequency synthesizers benefit from low phase noise and high output frequency but they are complex and expensive. DDS devices are cheaper and simpler but are limited by high spurious noise. Dr. Dai's novel DDS architecture effectively removes spurious noise, lowering it to levels comparable to analog synthesizers. In addition, the noise shaping allows for even finer frequency step size and even smaller silicon area. The Department of Defense has specifically requested these features in DDS designs and potential utility extends to commercial applications. This method can improve existing DDS devices, enable DDS to be used in applications currently dominated by analog devices (see [related Auburn BIST technology](#)), and improve remaining analog devices (e.g., by using DDS devices as a tunable reference in high frequency analog synthesizers).

Status

- U.S. patent number [7,577,695](#)
- This invention has been successfully verified by simulation (see figures)
- A DDS prototype with high-order $\Delta\Sigma$ interpolator in the phase domain to reduce the phase truncation error was fabricated and tested in a 0.35 μm CMOS technology [1].

Licensing Opportunities

- This technology is available for exclusive or non-exclusive licensing
- Joint development opportunities include funded research or a joint venture
- Related technology: [Automatic Analog BIST with Pattern Generator and Analyzer](#)

